Amendments to the Specification:

Please replace paragraphs [0020] and [0021] with the following amended paragraphs (in which deleted matter is shown with ~~strikethrough~~ text and in which added matter is shown underlined):

[0020] FIG. 2 is a block diagram of a configurable MUX 200 according to an exemplary embodiment of the present invention, which may be used as the configurable MUX 101. In this particular configuration, the AN signals include 32 signals distributed as the eight data I/O signals for each of four 8:1 MUXs 201, 202, 203 and 204, which include respective multiplexed I/O signals M1, M2, M3 and M4. The MUXs 201 - 204 each include or are otherwise coupled to a corresponding one of four 3:8 decoders 205, 206, 207 and 208, respectively. The decoders 205 - 208 each receive and decode three ADDR signals for selecting one of the eight data signals of its corresponding 8:1 MUX, as known to those skilled in the art, where the selected AN signal is asserted as the multiplexed (M) signal of the corresponding MUX or where the multiplexed signal is routed to the selected AN signal. For example, an ADDR of 000b (where "b" denotes a binary value) provided to the decoder ~~201b~~ 205 causes the MUX 201 to select its first data signal (e.g., signal 000b) to be coupled to the signal M1. The ADDR signals are a subset of the SEL signals from the digitization block 103.

[0021] The M1 - M4 I/O signals are coupled to a first interface of a switch matrix 209, which includes a second interface coupled to the SAN signals including individual signals SAN1, SAN2, SAN3 and SAN4 as shown. The switch matrix 209 includes eight single-pole, single-throw (SPST) switches S1, S2, S3, S4, S5, S6, S7 and ~~S7~~ S8, which are controlled by control (CTL) signals asserted by configuration logic 211. Each SPST switch is normally opened and closes upon receiving a corresponding control signal from the configuration logic 211. The switches S1-S3 each have one pole coupled to the M1 signal; the switches S4 and S5 each have one pole coupled to the M2 signal; the switches S6 and S7 each have one pole coupled to the M3 signal; and the switch S8 has one pole coupled to the M4 signal. The other pole of switch S1 is coupled to the SAN1 signal; the other pole of switches S2, S5, S7 and S8 are coupled to the SAN4 signal; the other pole of switches S3 and S4 are coupled to the SAN2 signal; and the other pole of the switch S6 is coupled to the SAN3 signal. In this manner, the SAN1 signal is selectively coupled to S1, the SAN2 signal is selectively coupled to S3 or S4, the SAN3 signal is selectively coupled to S6, and the SAN4 signal is selectively coupled to S2, S5, S7 or S8.